Laser-Crystallised Thin-Film Polycrystalline Silicon Solar Cells

Jonathon Dore
SPREE Research Seminar - 27th June, 2013
Contents

- Introduction – motivation for thin-film
- Thin-film PV technologies
- Diode laser crystallised thin-film pc-Si
  - Material and device preparation
  - Intermediate layers
  - Stability
  - Other current work
  - Near-term priorities for future work
  - Long-term priorities for future work
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1. Introduction

Development of Spot-Market Prices for Polysilicon (in US$ / kg)

GTM Research

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2. Thin-Film PV Technologies

- **Commercial**
  - CdTe
  - CIGS
  - a-Si/μc-Si

- **Research**
  - CZTS
  - OPV
  - Thin crystalline silicon
    - Wafer transfer
    - Thin polycrystalline
3. Thin Polycrystalline Si

- Solid Phase
  - SPC
  - AIC

- Liquid Phase
  - ZMR
  - EBC
  - LC
    - UV
    - Visible
    - IR
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4. Material Preparation

808 nm CW LIMO diode laser
12 mm x 170 µm

diffused n+
undoped poly-Si
B-doped Intermediate layer
Glass 5x5 cm²

~10 µm
~150 nm
3 mm
5. Grain structure

- Many $\Sigma 3$ twin boundaries
- Defect density $< 5 \times 10^7$ cm$^{-2}$
- Mobility of 300-450 at $\sim 1 \times 10^{16}$ cm$^{-3}$

Optical microscope

TEM

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6. Device Fabrication

- n contact pad
- Aluminium
- Resist
- n+
- p-
- Intermediate layer
- Glass
- p contact pad

Cell area = 1 cm²
7. Light IV

- $\eta = 11.7\%$
- $V_{OC} = 585\ mV$
- $J_{SC} = 27.6\ mA/cm^2$
- $FF = 72.4\ %$
8. Improvement path

Record Efficiency [%]


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8. Improvement path

Record Efficiency [%]

First devices with SiO$_x$ IL

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8. Improvement path

- First devices with SiO$_x$ IL
- SiO$_x$/SiC$_x$/SiO$_x$ IL

Record Efficiency [%]

<table>
<thead>
<tr>
<th>Month</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
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<tr>
<td>Jul</td>
<td>8.5</td>
<td>9.2</td>
<td>10.5</td>
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<td>Oct</td>
<td>7.8</td>
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<td>Jan</td>
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<td>Jul</td>
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</table>

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8. Improvement path

- **First devices with SiO\textsubscript{x} IL**
- SiO\textsubscript{x}/SiN\textsubscript{x}/SiO\textsubscript{x} IL
- SiO\textsubscript{x}/SiC\textsubscript{x}/SiO\textsubscript{x} IL

Record Efficiency [%]

- Jul-2011
- Oct-2011
- Jan-2012
- Apr-2012
- Jul-2012
- Oct-2012
- Jan-2013
- Apr-2013
- Jul-2013

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8. Improvement path

- First devices with SiO\textsubscript{x} IL
- SiO\textsubscript{x}/SiC\textsubscript{x}/SiO\textsubscript{x} IL
- SiO\textsubscript{x}/SiN\textsubscript{x}/SiO\textsubscript{x} IL
- improved SiO\textsubscript{x}/SiN\textsubscript{x}/SiO\textsubscript{x} IL; Rear texture

Record Efficiency [%]
Introduction – motivation for thin-film
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Diode laser crystallised thin-film pc-Si

– Material and device preparation
– Intermediate layers
– Stability
– Other current work
– Near-term priorities for future work
– Long-term priorities for future work
10. Intermediate Layer

Cell area = 1 cm²
10. Intermediate Layer

- Wetting layer
- Dopant source
- Contamination barrier
- Stable > 1414C
- Transparent anti-reflection coating (ARC)
- Passivation layer
11. Materials of Interest

- $\text{SiC}_x$
- $\text{SiN}_x$
- $\text{SiO}_x$

- Layers deposited by RF sputtering or PECVD
- 10-200 nm thick
- Either alone or in stacks
Intermediate Layer

- Wetting layer
- Dopant source
- Contamination barrier
- Stable > 1414C
- Transparent anti-reflection coating (ARC)
- Passivation layer
12. Wetting and crystallisation

- Laser energy

<table>
<thead>
<tr>
<th>Int. layer</th>
<th>Process range</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>13 J/cm²</td>
</tr>
<tr>
<td>SiO&lt;sub&gt;x&lt;/sub&gt;</td>
<td>194 J/cm²</td>
</tr>
<tr>
<td>SiN&lt;sub&gt;x&lt;/sub&gt;</td>
<td>220 J/cm²</td>
</tr>
<tr>
<td>SiO&lt;sub&gt;x&lt;/sub&gt;/SiC&lt;sub&gt;x&lt;/sub&gt; stack</td>
<td>246 J/cm²</td>
</tr>
</tbody>
</table>

Too low (nc regions)

Too high (dewetting)

Just right

Too low (nc regions)
13. Wetting and crystallisation

- Laser energy

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</tr>
<tr>
<td>SiN$_x$</td>
<td>220 J/cm²</td>
</tr>
<tr>
<td>SiO$_x$/SiC$_x$ stack</td>
<td>246 J/cm²</td>
</tr>
</tbody>
</table>

- SiN$_x$ layers result in pinholes in Si at high laser energies

Transmission micrograph
Intermediate Layer

- Wetting layer
- Dopant source
- Contamination barrier
- Stable > 1414C
- Transparent anti-reflection coating (ARC)
- Passivation layer
14. Dopant source

- **p**-poly-Si
- **Glass** 5x5 cm
- B-doped Intermediate layer
- SiOₓ/ SiNₓ/ SiOₓ stack
- Glass 5x5 cm²
15. Dopant source

- Uniform region created during molten phase
- $p^+$ region at interface?
16. Dopant source

- Spreading resistance shows no p+
- p+ region at interface?
- Inversion layer?
Intermediate Layer

- Wetting layer
- Dopant source
- Contamination barrier
- Stable > 1414°C
- Transparent anti-reflection coating (ARC)
- Passivation layer
17. Contamination Barrier

- Problem is blocking B from glass!
- \( \text{SiO}_x \) best barrier
- Can use \( \text{SiO}_x/\text{SiC}_x \) or \( \text{SiO}_x/\text{SiN}_x \) stacks

![Graph showing sheet conductance for different layers.](https://via.placeholder.com/150)
18. Contamination Barrier

- Iron can also diffuse from glass
- Iron found at silicon grain boundary when no IL used
- No iron when SiOx IL used
Intermediate Layer

- Wetting layer
- Dopant source
- Contamination barrier
- Stable > 1414C
- Transparent anti-reflection coating (ARC)
- Passivation layer
19. Stability

- Thick SiC<sub>x</sub> or SiN<sub>x</sub> layers cause wrinkling at the glass surface
- Visible in reflection micrographs at IL interface viewed through the glass

140nm SiC<sub>x</sub>  
80nm SiN<sub>x</sub>  
14nm SiC<sub>x</sub>  
80nm SiO<sub>x</sub>  
No IL
20. Stability

- Nitrogen from SiN$_x$ layer diffuses into Si during crystallisation
- N conc in Si when SiC$_x$ and SiO$_x$ used likely from atmosphere
- No excess C from SiC$_x$ or O from SiO$_x$
Intermediate Layer

- Wetting layer
- Dopant source
- Contamination barrier
- Stable > 1414°C
- Transparent anti-reflection coating (ARC)
- Passivation layer
21. Transparent ARC

- Ideally, $n = 2.4$, $d = \frac{\lambda_{\text{min}}}{4n}$
  and no absorption
22. Transparent ARC

- Ideally, \( n = 2.4, \quad d = \frac{\lambda_{\text{min}}}{4n} \)
  and no absorption
Intermediate Layer

- Wetting layer
- Dopant source
- Contamination barrier
- Stable > 1414C
- Transparent anti-reflection coating (ARC)
- Passivation layer
23. Passivation Layer

- Single- and double-layer stacks

- 80nm SiO$_x$ ($n \approx 1.5$)
- 20 nm SiC$_x$ ($n=2.9$) 80nm SiO$_x$
- 70 nm SiN$_x$ ($n=2.1$) 80nm SiO$_x$
24. Passivation Layer

- Poor front surface for $\text{SiO}_x/\text{SiC}_x$
25. Passivation Layer

- triple-layer stacks

15 nm SiO$_x$
20 nm SiC$_x$
80nm SiO$_x$

15 nm SiO$_x$
70 nm SiN$_x$
80nm SiO$_x$
26. Passivation Layer

- Surface SiOx improves IQE
- ONO still not ideal
26. Passivation Layer

- Surface SiOx improves IQE
- ONO still not ideal
- Optimised ONO (with reactive sputtering) better
26. Passivation Layer
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27. Stability

Baked | $J_{SC}$ mA/cm² | $V_{OC}$ mV | FF % | η %
-----|----------------|-------------|------|-----|
27.6  | 585            | 72.4        | 11.7 |
## Stability

<table>
<thead>
<tr>
<th>Condition</th>
<th>$J_{SC}$ mA/cm$^2$</th>
<th>$V_{OC}$ mV</th>
<th>FF (%)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baked</td>
<td>27.6</td>
<td>585</td>
<td>72.4</td>
<td>11.7</td>
</tr>
<tr>
<td>Degraded</td>
<td>27.7</td>
<td>572</td>
<td>62.9</td>
<td>10.0</td>
</tr>
</tbody>
</table>

![Graph showing current density vs. voltage for baked and degraded conditions](image-url)
28. Stability

- Occurs in dark
28. Stability

- Best stabilised efficiency = 10.4%
- Occurs in dark
- Related to absorber doping
- Days since first measurement

Best stabilised efficiency = 10.4%
29. Selective p+ (Chaho Ahn)

- Degradation likely due to poor contact with lightly-doped absorber

\[ p^- 10^{16} \text{ cm}^{-3} \]
29. Selective p+ (Chaho Ahn)

- Degradation likely due to poor contact with lightly-doped absorber
- Solution: selective p+ under absorber contact

\[ p^- \quad 10^{16} \text{ cm}^{-3} \]
### 30. Selective p+ (Chaho Ahn)

<table>
<thead>
<tr>
<th>Cell</th>
<th>$J_{sc}$ [mA/cm$^2$]</th>
<th>$V_{oc}$ [mV]</th>
<th>FF [%]</th>
<th>η [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline (initial)</td>
<td>23.6</td>
<td>524</td>
<td>62.3</td>
<td>7.7</td>
</tr>
<tr>
<td>Baseline (delayed)</td>
<td>23.9</td>
<td>434</td>
<td>46.4</td>
<td>4.7</td>
</tr>
<tr>
<td>Selective p+ (initial)</td>
<td>24.4</td>
<td>555</td>
<td>56.2</td>
<td>7.6</td>
</tr>
<tr>
<td>Selective p+ (delayed)</td>
<td>24.2</td>
<td>559</td>
<td>56.9</td>
<td>7.7</td>
</tr>
</tbody>
</table>

- Data for cells with SiO$_x$ intermediate layer
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31. Rear Texture (Zamir Pakhuruddin)
32. Rear Texture (Zamir Pakhuruddin)

AFM
RMS = 78 nm

Absorption without rear reflector or ARC
33. Rear Texture (Zamir Pakhuruddin)
33. Rear Texture (Zamir Pakhuruddin)
34. Suns-$V_{oc}$

- Measured after metallisation
  - Significant $R_{SH} \sim 500$ Ohms.cm$^2$ and $n = 2$ influence

---

Measured

Fit

$n=1$

$n=2$

Shunt

Voltage [V]

Suns

0.3 0.4 0.5 0.6 0.7

0.01 0.1 1 10
35. Dark Lock-In Thermography

- DLIT shows hotspot at Si crack (shown for neighbouring cell)
- Same in forward and reverse bias
  - Ohmic shunt
36. Crack-free crystallisation (Jialiang Huang)

**Standard process**

**“Crack-free” process**

Scan direction

12 mm

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37. Grain orientation control (Jae Sung Yun)

![Inverse pole orientation map](image)

- **Position 1**
  - Standard Process
  - 100 nm SiO$_x$ Capping Layer

- **Position 2**

- **Position 3**
  - Inverse pole orientation map
38. Laser diffusion (Miga Jung)

- **RTP diffusion**
  - Expensive
  - Slow
  - Causes glass softening
  - Exacerbates cracks
  - Large process window?

- **Laser diffusion**
  - Cheap
  - Fast
  - No effect on glass
  - No effect on cracks
  - Process window?

![Graph showing sheet resistance comparison between RTP and Laser diffusion samples.](image-url)
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39. Near-Term Priorities for Future Work

- Transfer processes to TETB
- Improve bulk passivation
- Improve surface passivation
- Identify and address device fabrication losses
  - E.g. Cell isolation scribes

- Investigate alternative junction formation
  - Heterojunction
  - Other?

- Plasmonic light-trapping?
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40. Simple economics

* Multi wafer spot price = $0.84/wafer
  @ eff = 17% → $0.20/W

* BSG ~ $20/m² above standard glass
  @ eff = 12% → $0.17/W

* Need to increase eff and/or use standard glass
41. Process sequence

- **Typical TF-Si**
  - Clean
  - Deposit
  - Scribe
  - Clean
  - Deposit
  - Scribe
  - Module assembly

- **Laser-crystallised TF-Si**
  - Clean
  - Deposit
  - Crystallise
  - Coat
  - Diffuse
  - Etch
  - Hydrogenate
  - Scribe
  - Coat
  - Bake
  - Inkjet
  - Etch
  - Expose
  - Bake
  - Inkjet
  - Clean
  - Bake
  - Clean
  - Deposit
  - Scribe
  - Bake
  - Module Assembly

- Need to simplify contacting scheme
42. Conclusions

- Laser-crystallised poly-Si solar cell reaching 11.7% efficiency
  - Exceeds record for thin-film poly-Si
- Short-term, recoverable degradation
- Selective p+ metallisation makes stable cells
- Performance improvements mostly due to intermediate layer
- Many more opportunities for further improvement